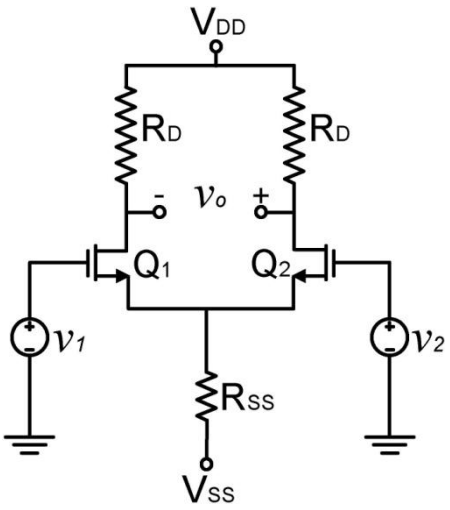
LO-7

To Do The Analysis and Design of Differential Amplifiers

1. For the given circuit; V_{DD} =12 V, V_{SS} =-12 V, R_{SS} =220 kΩ, R_D =330 kΩ, $\mu_n C_{ox}(W/L)$ =0.4 mA/V^2, V_{TN} =1 V



a) Find the DC drain current (I_D) and the small signal parameter g_m of the Q_1 transistor.
b) Find the differential-mode gain.
c) Find the common-mode gain.
d) Find CMRR
e) If v_1 = 0.1 sin(2π*60t) + 0.005 sin(2π*1000t), v_2 = 0.1 sin (2π*60t) - 0.005 sin(2π*1000t) volts, then find v_o.

2. Consider the differential amplifier given in the figure below.

V_{DD} = 2.5 V, V_{SS} = 2.5 V, R_D = 20 kΩ,
$(W/L)_1$ = 20/1, $(W/L)_2$ = 2/1, $(W/L)_3$ = 4/1,
$(W/L)_4$ = $(W/L)_5$ = 10/1,

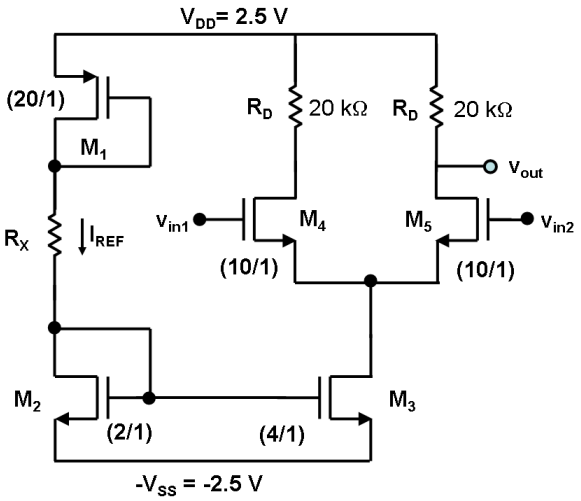
For all nMOS transistors:

K_n' = 50 μA/V^2, V_{tn} = 1 V, λ = 0.01 V^{-1}

For all pMOS transistors:

K_p' = 25 μA/V^2, V_{tp} = -1 V, λ = 0.01 V^{-1}

Assume that all MOS transistors are in SAT.



a) Determine the value of R_X to set I_{REF} = 100μA. Determine the drain current values for transistors M_4 and M_5.

For the rest of the problem, assume that I_{REF} = 100μA

b) Find the single-ended output differential gain A_d
c) Find the single-ended output common-mode gain A_c.
d) Find the Common-Mode Rejection Ratio (CMRR) for both single-ended output and differential output cases.
e) Find the common-mode input range (*Maximum* and *Minimum* common-mode input voltages for proper operation) for this amplifier.

3. Consider the following differential pair. A design error has resulted in a gross mismatch in the W/L ratios, i.e., Q_2 has twice the W/L ratio of Q_1; i.e., $(W/L)_2 = 2\ (W/L)_1$

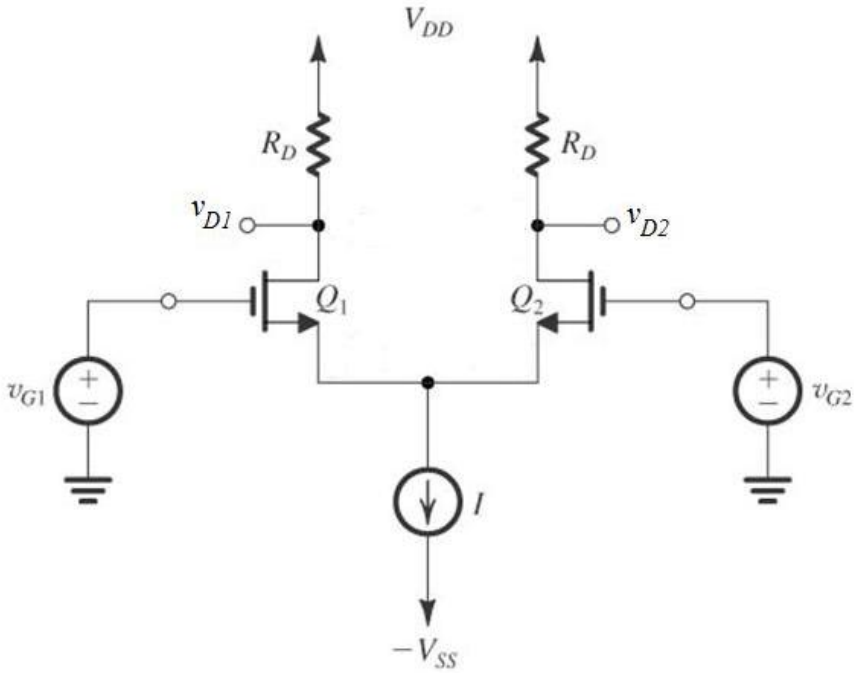
(a) Determine the dc drain currents I_{D1} and I_{D2} in terms of the biasing current source I.

(b) Calculate the overdrive voltages $V_{ov} = V_{GS}-V_t$ and transconductances g_{m1}, g_{m2} for each of Q_1 and Q_2 in terms of I and transistor parameters.

(c) Draw the small-signal model of the differential amplifier circuit.

(d) Determine the differential gain $A_d = (v_{d2}-v_{d1})/v_{id}$ in terms of R_D and transconductances of the transistors.

(e) What is the input-referred dc offset voltage V_{os} of this amplifier?



4. For the circuit given in Figure 1,

a) Find the value of $\mathbf{R_X}$ to set $\mathbf{I_{REF}=0.1mA.}$

b) Determine the values of $\mathbf{I_X}$, $\mathbf{I_Y}$, **and** $\mathbf{I_Z}$ currents.

c) Draw the differential and common-mode half circuits.

d) Find the **differential** voltage gain

$$\mathbf{A_d=(v_{out1}-v_{out2})/(v_{in1}-v_{in2}))}$$

and the **common-mode** voltage gain

$$\mathbf{(A_{cm}=v_{out1}/v_{cm})}\ .$$

e) Find the **Common-Mode-Rejection-Ratio (CMRR)** for <u>both single-ended and differential output case</u>.

f) Determine the input offset voltage for **1% mismatch** in the **load resistances ($\mathbf{R_D}$)**.

g) Determine the **CMRR** for **1% mismatch** in the **load resistances ($\mathbf{R_D}$)**.

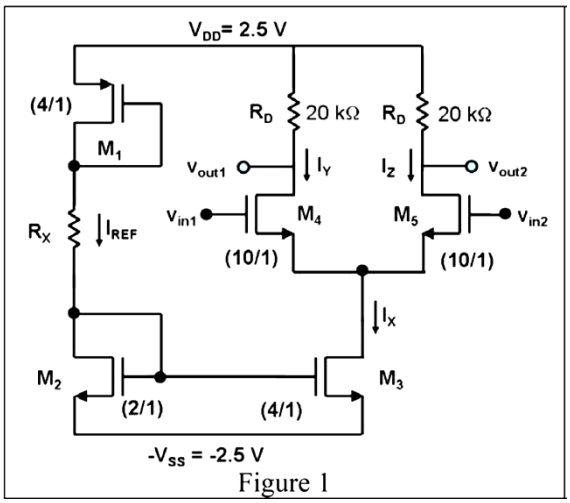


Figure 1

Transistor Parameters:

K_n'=100 μA/V^2, K_p'=50 μA/V^2,

V_{TN}=1V, V_{TP}=-1V, and $\lambda_n=\lambda_p$=0.02 V^{-1}.

5. For the circuit given in Figure 2,

a) Find **the differential mode voltage gain.**

b) Determine the **common mode voltage gain**.

c) If $\mathbf{v_{in1}}$ = 0.1 sin(2π*60t) + 0.005 sin(2π*1000t),

$\mathbf{v_{in2}}$ = 0.1 sin (2π*60t) - 0.005 sin(2π*1000t) volts,

then find $\mathbf{v_{out1}}$ and $\mathbf{v_{out2}}$.

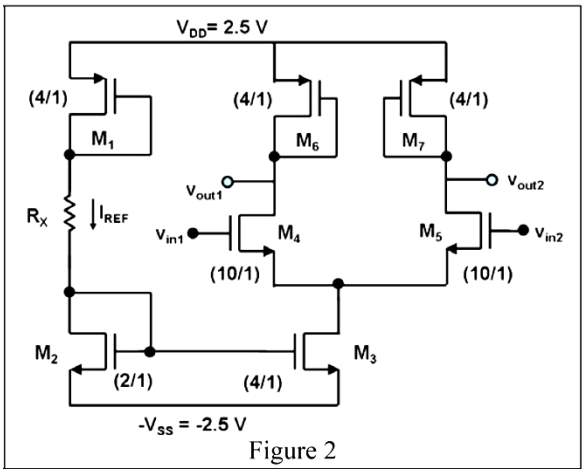


Figure 2

Transistor Parameters:

K_n'=100 μA/V^2, K_p'=50 μA/V^2,

V_{TN}=1V, V_{TP}=-1V, and $\lambda_n=\lambda_p$=0.02 V^{-1}.

6. This problem deals with the differential amplifier shown on the figure given on the right.

Assume that all transistors are in <u>forward active region</u>.

Assume also that the input signals (v_{in1} and v_{in2}) have zero <u>DC</u> voltage components.

a) Find the values of $\mathbf{I_{REF}}$, $\mathbf{I_1}$, and $\mathbf{I_2}$.

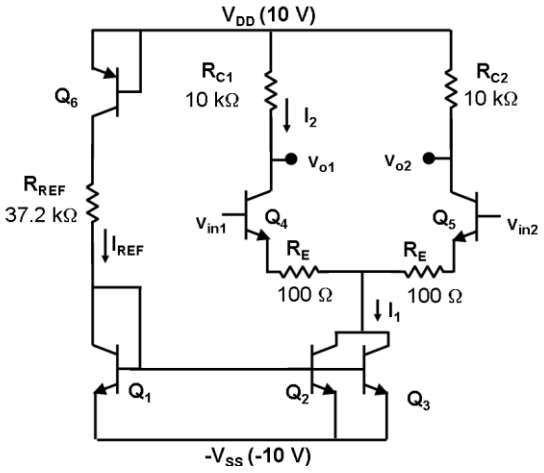
b) Draw the **differential** and **common-mode** <u>*small-signal*</u> half circuits for the amplifier.

c) Find the **differential gain** of the amplifier $\left(\frac{v_{o1}-v_{o2}}{v_{in1}-v_{in2}}\right)$.

d) Find the **common-mode gain** of the amplifier <u>for both single-ended and differential output cases</u>.

e) Find the **common-mode rejection ratio (CMRR)** of this amplifier <u>in dB for both single-ended and differential output cases</u>.

f) Assume that there is a mismatch between R_{C1} and R_{C2}, and due to this mismatch $\mathbf{R_{C1}=10\ k\Omega}$ and $\mathbf{R_{C2}=10.1\ k\Omega}$. What is the **CMRR** for this mismatch?



Transistor Parameters

Q_4 and Q_5: $V_A = \infty$

Q_1, Q_2, Q_3, and Q_6: V_A = 100 V

Q_1, Q_2, Q_3, Q_4, and Q_5: $V_{BE(on)}$ = 0.7V

Q_6: $V_{EB(on)}$ = 0.7V

Q_1, Q_2, and Q_3 are identical.

Q_4 and Q_5 are identical.

V_T=25mV @ 300K